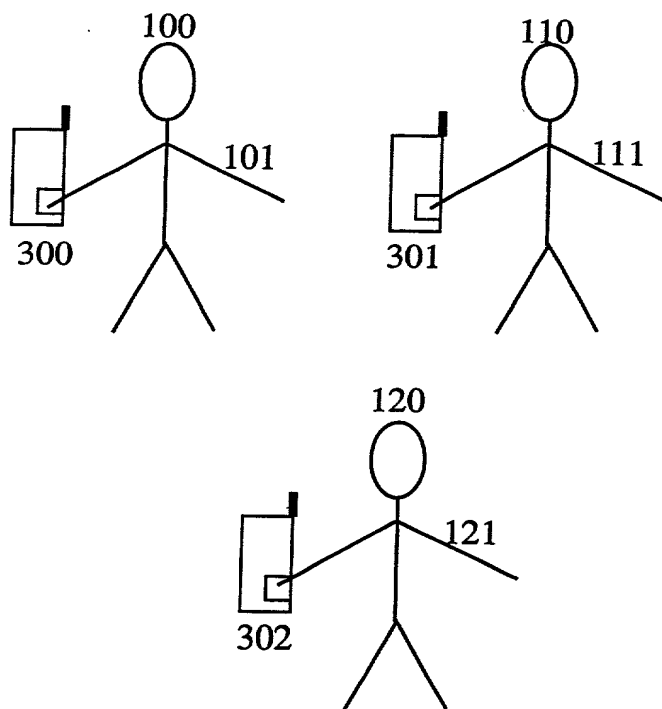
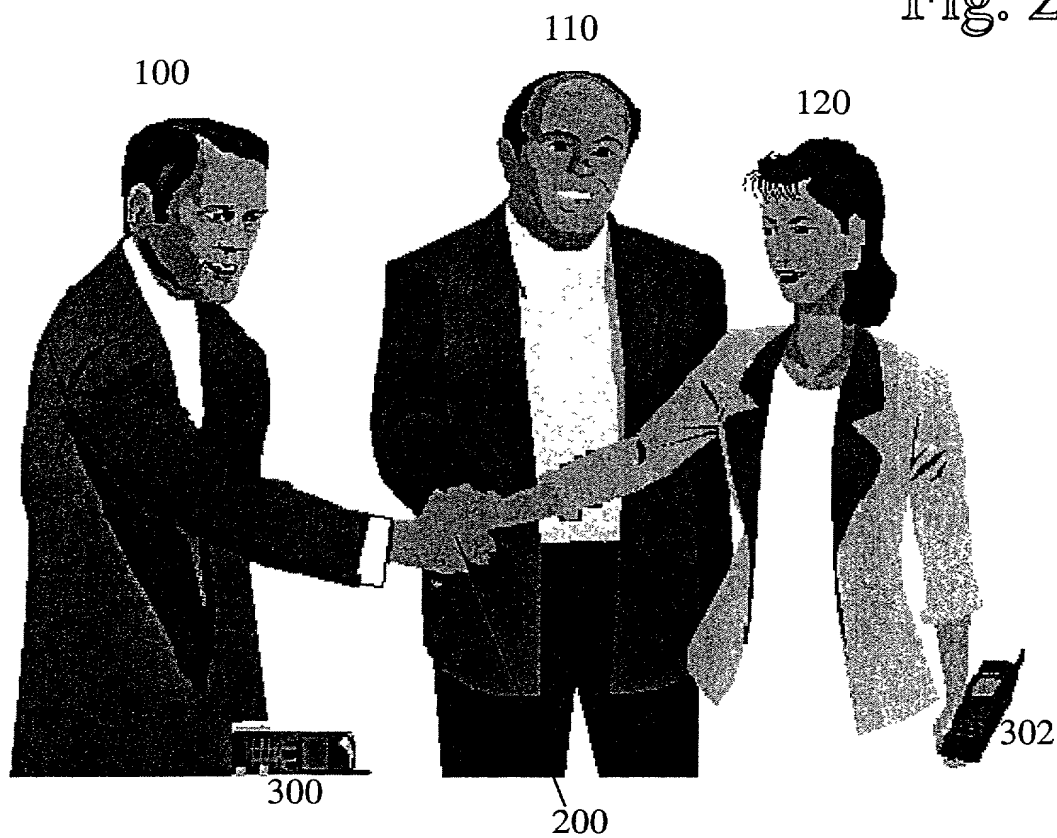


Fig. 1



10027501.041502

Fig. 2



10027501.041502

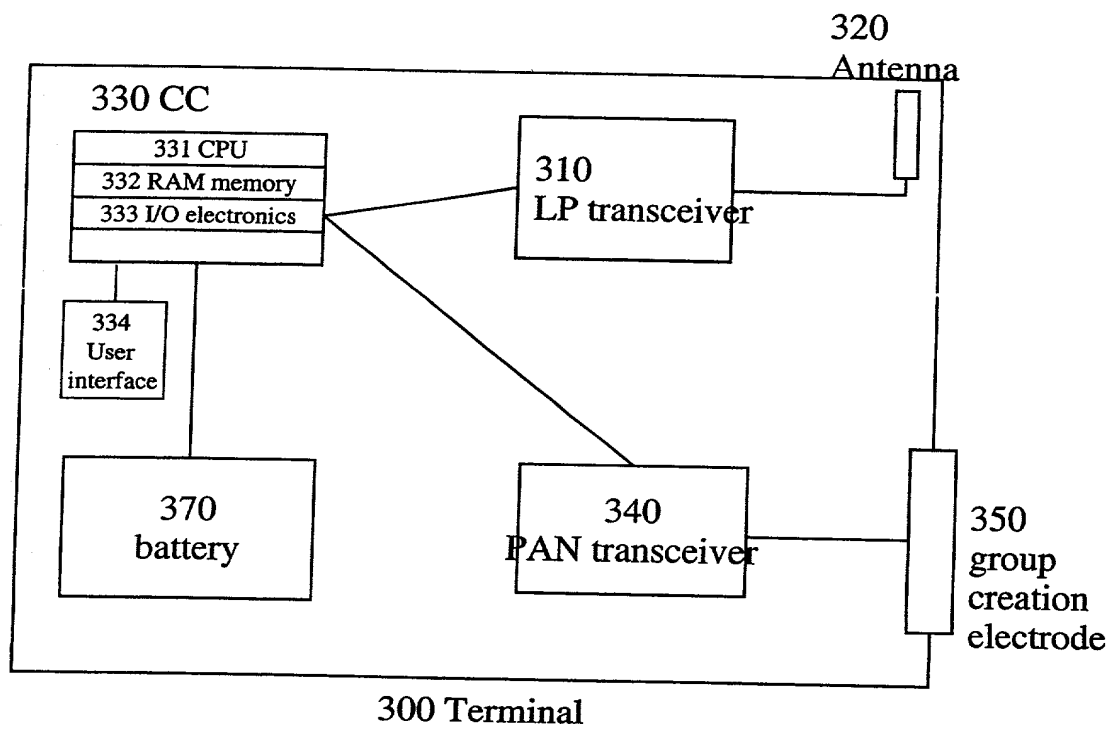


Fig. 3

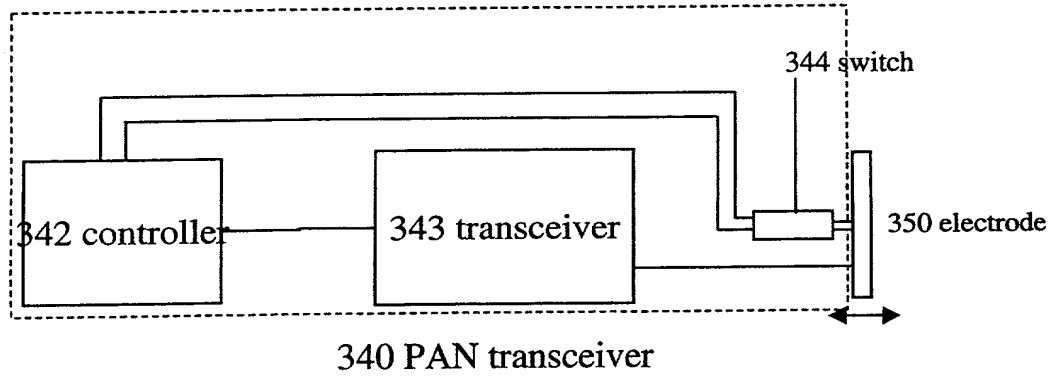


Fig. 4A

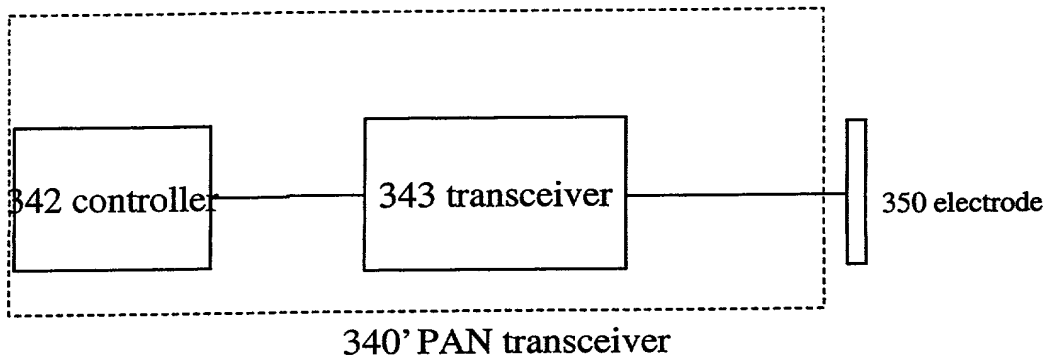


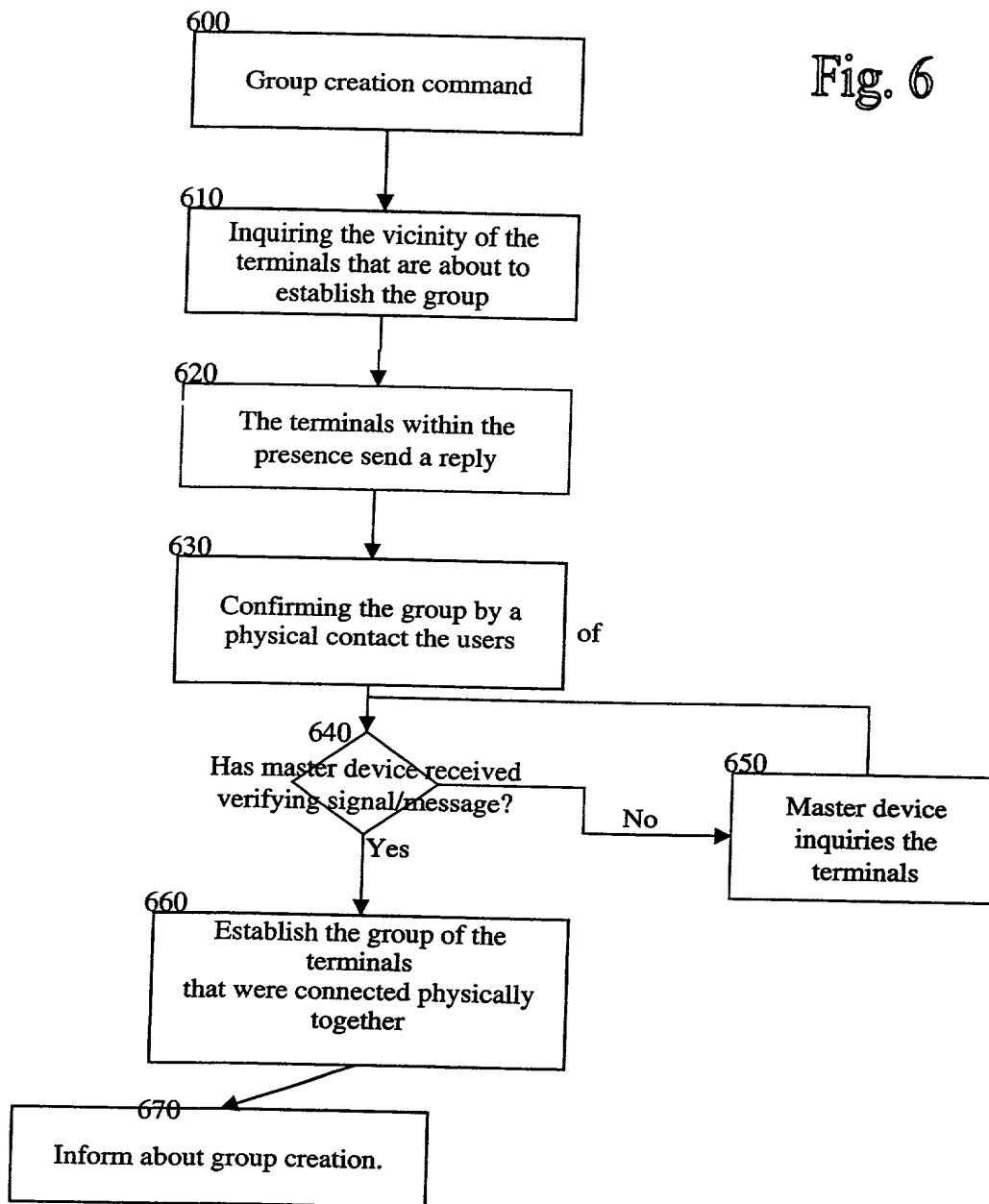
Fig. 4B

10027501.04300
2009-10-20 10:20:00

501	502	503
BD_ADDR	Clock Offset	Class of Device

Fig. 5

Fig. 6



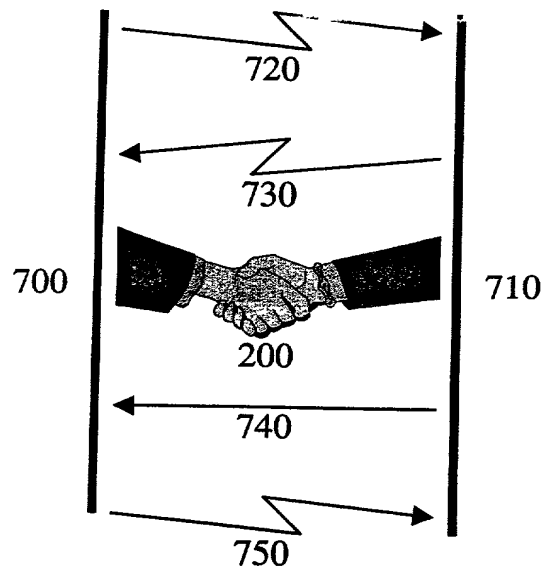


Fig. 7

10027501.041502

Fig. 8

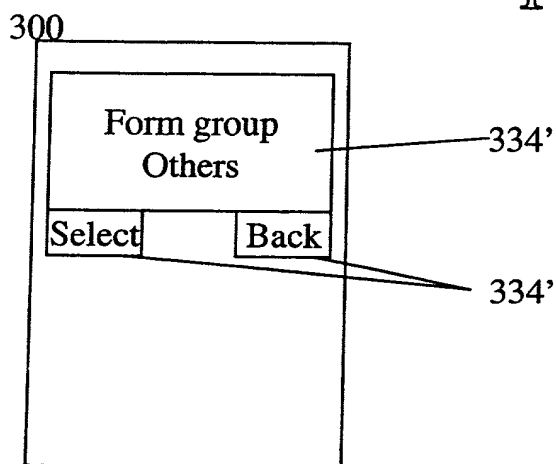
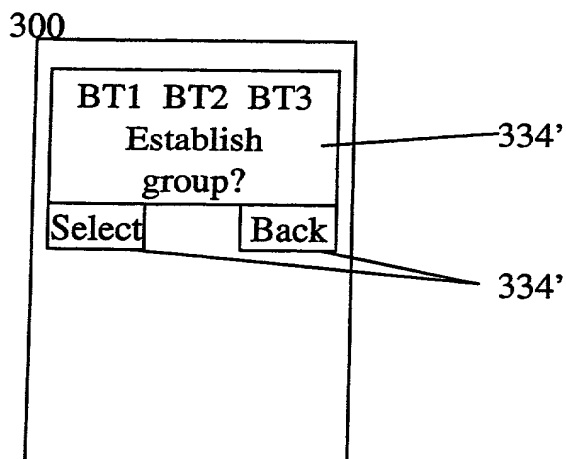


Fig. 9



10027501.04.1502
2005140" T05/22007